S/N 08/902,133 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes et al.
Examiner: Valencia Wallace
Serial No.: 08/902,133
Group Art Unit: 2815
Filed: July 29, 1997
Docket: 303.356US1
Title: DYNAMIC ELECTRICALLY ALTERABLE PROGRAMMABLE READ ONLY MEMORY DEVICE

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

When the above-identified patent application is taken up for consideration, please amend the application as follows:

IN THE CLAIMS

Please amend the following claims:

18.(Three times amended) The transistor of claim 28, wherein [the] an area of a capacitor formed by the control electrode, the floating gate, and the intergate dielectric is larger than [the] an area of a capacitor formed by the floating gate, the insulator, and the channel region.

19.(Twice Amended) A transistor comprising:

a source region;

a drain region;

a channel region between the source region and the drain region; [and]

a floating gate separated from the channel region by an insulator, wherein a barrier energy between the floating gate and the insulator is less than approximately 3.3 eV;

a control electrode, separated from the floating gate by an intergate dielectric; and

wherein the intergate dielectric has a permittivity that is higher than a permittivity of silicon dioxide.

29.(Amended) A memory cell comprising:

a storage electrode [for storing] to store charge;

a control electrode, separated from a storage electrode by an intergate dielectric; and